

Notice of References Cited	Application/Control No. 09/728,441	Applicant(s)/Patent Under Reexamination HWU ET AL.	
	Examiner Aimee J Li	Art Unit 2183	Page 1 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,085,315	07-2000	Fleck et al.	712/241
	B	US-5,867,711	02-1999	Subramanian et al.	717/161
	C	US-6,421,744	07-2002	Morrison et al.	710/22
	D	US-5,835,776	11-1998	Tirumalai et al.	717/161
	E	US-5,809,308	09-1998	Tirumalai, Partha P.	717/161
	F	US-5,664,193	09-1997	Tirumalai, Partha P.	717/153
	G	US-5,579,493	11-1996	Kiuchi et al.	712/207
	H	US-6,598,155	07-2003	Ganapathy et al.	712/241
	I	US-6,269,440	07-2001	Fernando et al.	712/241
	J	US-6,367,071	04-2002	Cao et al.	717/160
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Madhavi Gopal Valluri and R. Govindarajan. "Modulo-Variable Expansion Sensitive Scheduling". High Performance Computing, 1998. HIPC '98. 5th International Conference on, 17-20 December 1998. Pages 334-341.
	V	InstantWeb. Online Computing Dictionary. Search term: interrupt □□http://www.instantweb.com/foldoc/foldoc.cgi?query=interrupt
	W	P. Tirumalai, M. Lee, and M. Schlansker. "Parallelization of Loops with Exits on Pipelined Architectures". Supercomputing '90. Proceedings of, 12-16 November 1990. Pages 200-212.
	X	Uma Mahadevan, Kving Nomura, Roy Dz-ching Ju, and Rick Hank. "Applying Data Speculation in Modulo Scheduled Loops". Parallel Architectures and Compilation Techniques, 2000. Proceedings. International Conference on, 15-19 October 2000. Pages 169-176.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.